POTENTIAL AND DRAIN CURRENT SIMULATION OF A SYMMETRIC DOUBLE GATED MOLYBDENUM DISULFIDE (MOS2) TRANSISTOR

R. Sridevi

Assistant Professor, Department of Electronics and Communication Engineering, M.Kumarasamy College of Engineering, Karur (India). E-mail: sridevir.ece@mkce.ac.in ORCID: https://orcid.org/0000-0003-300-3336

J. Charles Pravin

Associate Professor, Centre for VLSI Design, Department of Electronics and Communication, Kalasalingam Academy of Research and Education. Virudhunagar (India). E-mail: charles@klu.ac.in ORCID: https://orcid.org/0000-0002-9009-6274

Recepción: 28/11/2019 Aceptación: 04/12/2020 Publicación: 30/11/2021

Citación sugerida:

Sridevi, R., y Pravin, J. C. (2021). Potential and drain current simulation of a symmetric double gated Molybdenum Disulfide (MoS2) transistor. *3C Tecnología. Glosas de innovación aplicadas a la pyme, Edición Especial*, (noviembre, 2021), 385-395. https://doi.org/10.17993/3ctecno.2021.specialissue8.385-395

ABSTRACT

As the scaling of silicon MOSFET reaches its physical limit, research efforts have been made in exploring alternative devices. In this paper, we have examined the enhanced drain current, electrostatic potential, mobility, and electric field for a symmetric structure of Double gated Molybdenum Disulfide (MoS_2) transistor. The performance of the device has been simulated using Technology Computer-Aided Design (TCAD) simulation tool. The above mentioned comparison model of drain current built by use of symmetric Double gated MoS_2 transistor has shown superior performances when compared with that of Silicon transistor. There is an enhancement of 0.1 µA in its drain current and the mobility is 50 higher than the silicon based transistor, under the condition that this device has the same geometry. It was performed by incorporating the quantum mechanical effects in molybdenum disulfide (MoS_2) based transistor. Due to its high performance in low power operating voltages, MoS_2 transistor will be suitable for low power applications.

KEYWORDS

2D material, MoS₂, Drain Current, FET, TCAD Simulation tool.

1. INTRODUCTION

In the recent decade, silicon-based transistor has reached its scaling limit. Hence, researchers have been discovering solutions for finding alternative channel materials for future semiconductor devices; such has the transition metal dichalcogenides (TMDs) material of MoS₂, which is chosen due to their high ON- OFF ratio and mobility. Unlike graphene, MoS₂ material has large bandgap of 1.23 eV, so it can be easily turned off. Compared to Silicon dioxide, high k dielectric materials are mostly preferred because of its reduced threshold voltage and improve current ON/OFF ratio (Ajayan *et al.*, 2017; Pravin *et al.*, 2016; Boucart & Ionescu, 2007).

We present the simulated result of drain current, electrostatic potential, mobility, and electric field for symmetric double gated MoS_2 transistor using Technology Computer-Aided Design (TCAD) simulation tool. Here we have been used the drift diffusion model is the carrier transport model in Sentaurus Device ("SentaurusTM Device User Guide. Version K-2015.06", 2015). Based on the literature survey (Pravin *et al.*, 2016b; Pravin *et al.*, 2018; Semiconductor Industry Association, 2015; Tiwari *et al.*, 2017), our numerical model has been simulated. Finally, we have to extract the physical parameters of drain current, electrostatic potential, mobility, and electric field for MoS_2 based transistor by TCAD simulation tool. We have to compare the obtained results of MoS_2 material and silicon material, where our proposed model has shown the higher performance.

In this paper, we address a symmetric Double gated MoS_2 transistor, it produces the higher drain current compared to Single gate MoS_2 transistor.

2. MATERIALS AND METHODS

The physical structure of symmetric Double gated MoS_2 based transistor is presented in Figure 1, which has been modeled with channel length (Lch) of 20 nm, 10 nm thickness of the gate oxide (tox), and channel thickness (tch) of 10 nm (Jiang *et al.*, 2015). These values are shown in Table 1.

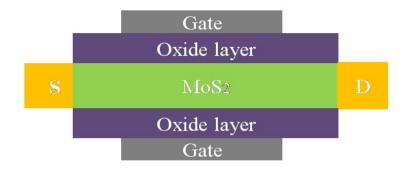


Figure 1. Device geometry of symmetric Double gated MoS_2 transistor. Source: own elaboration.

Table 1. Values of the physical structure of the double-gate MoS₂-based symmetric transistor.

Parameters	Values
Channel Length	20 nm
Gate Oxide	10 nm
Channel thickness	10 nm
Drain/Source Doping	1e18
Channel Doping	1e ²¹
MoS ₂ band gap	1.23 eV

Source: own elaboration.

The Drift diffusion model and Shockley Read Hall Recombination model have been used in the simulation for determine the drain current of proposed device ("Sentaurus[™] Device User Guide. Version K-2015.06", 2015).

DRIFT-DIFFUSION MODEL:

In Sentaurus Device, the default carrier transport model of drift-diffusion model is used. The electron current density and hole current density are given below,

$$\vec{J_n} = \mu_n (n \nabla E_c - 1.5 n k T \nabla ln m_n) + D_n (\nabla_n - n \nabla ln \gamma_n)$$
$$\vec{J_p} = \mu_p (p \nabla E_v - 1.5 p k T \nabla ln m_p) + D_p (\nabla_p - n \nabla ln \gamma_p)$$

Due to spatial variations of the electron affinity, the electrostatic potential and the band gap. These terms are taken into the report the contribution. The remaining terms of effective masses of m_n and m_p are taken into the report the contribution due to the spatial variation and the gradient of concentration.

By using Einstein relation, the diffusivities D_n and D_p are derived through the mobilities.

$$D_n = kT\mu_n and D_p = kT\mu_p$$

SCHOCKLEY-READ-HALL RECOMBINATION:

In Sentaurus Device, Schockley-Read-Hall (SRH) recombination model is achieved:

$$R_{net}^{SRH} = \frac{np - n_{i,eff}^2}{\tau_p(n+n_1) + \tau_n(p+p_1)}$$
$$n_1 = n_{i,eff} \exp\left(\frac{E_{trap}}{KT}\right)$$
$$p_1 = n_{i,eff} \exp\left(\frac{-E_{trap}}{KT}\right)$$

The difference between the detect level and intrinsic level is termed as E_{trap} .

SRH DOPING DEPENDENCE:

In Sentaurus Device, the doping dependence of the SRH lifetimes is modeled with the help of Scharfetter relation:

$$\tau_{dop} (N_{A,0} + N_{D,0}) = \tau_{dop} + \frac{\tau_{max} - \tau_{min}}{1 + \left(\frac{N_{A,0} + N_{D,0}}{N_{ref}}\right)^{\gamma}}$$

When the argument Doping Dependence is particularized for the SRH Recombination, where the Scharfetter relation is used.

3. RESULTS

Based on the equations obtained for Drift-Diffusion model and Schockley-Read-Hall Recombination was carried out in the MoS_2 structure for finding the drain current, electrostatic potential, mobility, and electric field.

The final results show that the proposed MoS_2 device structure displayed improved performances in terms of both drain current as well as mobility than the silicon transistor.

3.1. SIMULATION RESULT OF DRAIN CURRENT

The MoS_2 channel material based transistor device is simulated with drift diffusion model in Sentaurus Device. Figure 2 depicts the analyzation of the drain current of the transistor device. The obtained result produces higher drain current at 1 V of gate voltage for short channel length device. This result illustrates that the MoS_2 material produces higher drain current compared to silicon material. When we are applied high gate voltages it reaches the high drain current.

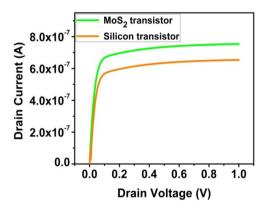


Figure 2. Comparison of drain current for MoS_2 material and Silicon material. Source: own elaboration.

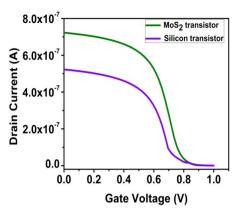


Figure 3. Comparison of drain current for MoS_2 material and Silicon material. Source: own elaboration.

Figure 3 shows the output characteristics of drain current for MoS_2 material and silicon material. This result depicts the drain current with the function of gate voltage at 1 V of drain voltage.

3.2. SIMULATION RESULT OF ELECTRIC FIELD

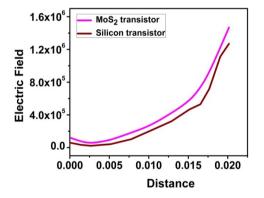


Figure 4. Analyzation of electric field for MoS_2 material and Silicon material. Source: own elaboration.

Figure 4 shows the electric field for MoS_2 material and silicon material. This result depicts the electric field for MoS_2 produces a higher value tan the silicon transistor.

3.3. SIMULATION RESULT OF MOBILITY

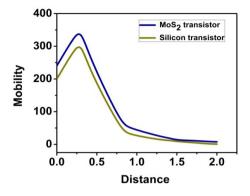


Figure 5. Mobility for ${\rm MoS}_2$ material and Silicon material. Source: own elaboration.

3.4. SIMULATION RESULT OF POTENTIAL

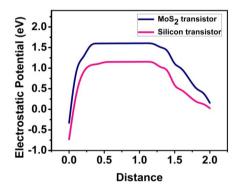


Figure 6. Comparison of electrostatic potential for MoS_2 material and Silicon material. Source: own elaboration.

The above figure shows the mobility, and electrostatic potential for a symmetric structure of double gated MoS_2 transistor. The heavy doping of body makes difficult the potential calculation. To overcome this constraint, using Poisson equation in existence of important body doping. The electrostatic potential is achieved by solving Poisson equation.

4. CONCLUSIONS

This paper introduced a MoS_2 based transistor with high k dielectric material, which has merits in terms of device performance of the reduced threshold voltage. A performance evaluation was done for the MoS_2 based transistor for finding out the drain current, electrostatic potential, mobility, and electric field. The performance of the device has been simulated using Technology Computer-Aided Design (TCAD) simulation tool. The above mentioned comparison model of drain current built by use of symmetric Double gated MoS_2 transistor has shown superior performances when compared with that of Silicon transistor. There is an enhancement of 0.1 µA in its drain current and the mobility is 50 higher than the silicon based transistor, under the condition that this device has the same geometry. It was performed by incorporating the quantum mechanical effects in molybdenum disulfide (MoS_2) based transistor. We have successfully investigated the MoS_2 material based transistor and its characteristics.

ACKNOWLEDGEMENT

The authors are grateful to centre for VLSI Design, Department of Electronics and Communication Engineering, Kalasalingam Academy of Research and Education (KARE) for supporting this research.

REFERENCES

- Ajayan, J., Nirmal, D., Prajoon, P., & Pravin, J. C. (2017). Analysis of nanometer-scale InGaAs/InAs/InGaAs composite channel MOSFETs using high-K dielectrics for high speed applications. AEU - International Journal of Electronics and Communications, 79, 151-157. http://doi.org/10.1016/j.aeue.2017.06.004
- Boucart, K., & Ionescu, A. M. (2007). Double-Gate Tunnel FET With High- Gate Dielectric. IEEE Electron Device Letter, 54(7), 1725-1733. https://doi.org/10.1109/ TED.2007.899389

- Cao, J., Liu, W., Wu, Q., Yang, G., Lu, N., Ji, Z., Geng, D., Li, L., & Liu, M. (2018). A New Velocity Saturation Model of MoS2 Field-Effect Transistors. *IEEE Electron Device Letter*, 39(6), 893-896. https://doi.org/10.1109/LED.2018.2830400
- Jiang, C., Liang, R., Wang, J., & Xu, J. (2015). A two-dimensional analytical model for short channel junctionless double-gate MOSFETs. AIP Advances, 5, 057122. https:// doi.org/10.1063/1.4921086
- Pravin, J. C., Nirmal, D., Prajoon, P., & Ajayan, J. (2016a), Implementation of nanoscale circuits using dual metal gate engineered Nanowire MOSFET with high-k dielectrics for low power applications. *Physica E: Low-dimensional Systems and Nanostructures*, 83, 95-100. http://doi.org/10.1016/j.physe.2016.04.017
- Pravin, J. C., Nirmal, D., Prajoon, P., & Menokey, M. A. (2016b). A New Drain Current Model for a Dual Metal Junctionless Transistor for Enhanced Digital Circuit Performance. *IEEE Transactions on Electron Devices*, 63(9), 3782-3789. https:// doi.org/10.1109/TED.2016.2591982
- Pravin, J. C., Prajoon, P., Nesamania, F. P., Srikesh, G., Kumar, P. S., & Nirmal D. (2018). Nanoscale High-k Dielectrics for Junctionless Nanowire Transistor for Drain Current Analysis. *Journal of Electronic Materials*, 47(5), 2679-2686. http://doi. org/10.1007/s11664-018-6075-2
- Ryu, J. H., Baek, G.-W., Yu, S. J., Seo, S. G., & Jin, S. H. (2017). Photosensitive Full-Swing Multi-Layer MoS2 Inverters with Light Shielding Layers. *IEEE Electron Device Letters*, 38(1), 67-70. https://doi.org/10.1109/LED.2016.2633479
- Semiconductor Industry Association. (2015). *ITRS version 2.0.* http://www.semiconductors.org/main/2015_international_technology_roadmap_for_semiconductors_itrs/
- Sentaurus[™] Device User Guide. Version K-2015.06. (2015). Synopsys. http://www.sentaurus. dsod.pl/manuals/data/sdevice_ug.pdf
- Tiwari, S., Dolai, S., Rahaman, H., & Gupta, P. S. (2017). Effect of Temperature and phonon scattering on the Drain current of a MOSFET using SL-MoS2 as its channel

material. Superlattices and Microstructures, 111, 912-921. https://doi.org/10.1016/j. spmi.2017.07.051