THERMAL AND CONGESTION AWARE ALGORITHM FOR 3D INTEGRATED CIRCUITS

Pandiaraj Kadarkarai

Department of ECE, Kalasalingam Academy of Research and Education, Tamil Nadu, (India).

E-mail: pandiaraj@klu.ac.in

ORCID: https://orcid.org/0000-0001-9610-2172

Sivakumar Pothiraj

Department of ECE, Kalasalingam Academy of Research and Education, Tamil Nadu, (India).

E-mail: siva@klu.ac.in

ORCID: https://orcid.org/0000-0003-1328-8093

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ABSTRACT

In VLSI physical Design methodology, Routing has been a most important in VLSI design, because the routing results are like circuit delay, power consumption, chip responsibility and manufacturability etc. With the advancements in 3D ICs, this issue has turned out to be substantially more complex. With the size of present-day plans at a huge number of nets, global routing has turned into a noteworthy computational test. The main purpose of the global routing is to reduce the wire length. In this work, a thermal and congestion aware formula is projected to attenuate the mixture wire length and to beat the congestion by systematically diffusive the nets within the routing region. The investigational output of the planned global router utilizes less wirelength and keeps far from congestion by ripping up and re-routing the nets. In future planned to use machine learning algorithm to reduce temperature between the layers in an integrated circuit.

KEYWORDS

Global Routing, NP completeness, 3D ICs, Wire Length Minimization, Congestion.

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1. INTRODUCTION

VLSI physical outline is the way toward deciding the physical area of dynamic gadgets and interconnecting them inside the limit of a VLSI chip. Physical configuration of a circuit is the stage that goes before the manufacture of a circuit. For the most part, it alludes to all union strides succeeding rationale plan and going before manufacture. The physical outline systems intend to create designs with a little region, high flag respectability, diminished postponement, decreased force utilization and higher yield. Physical design phases include partitioning, floor planning, placement, clock-tree synthesis and routing as shown in Figure 1.

Execution of VLSI circuits is in effect to a great extent overwhelmed by the between interfaces because of diminishing wire pitch and expanding bite the die size. Issue is additionally testing a 3D IC due to the distance of elements. It in the end builds the significance of global routing issue which makes it all the more difficult. Advanced methods are utilized for global routing frequently. The most recent looks into on global routing is meant to upgrade diverse multi-target capacities related with execution and blockage, warm issues (Goplen & Sapatnekar, 2005), obstruction (Minz, Wong, & Lim, 2005), impediment mindful steering (Pandiaraj *et al.*, 2017a; Ghosal, Das, & Das, 2012b) and so forth.

3D Integration offers an assortment of points of interest for future VLSI configuration, similar to 1) higher packing thickness and littler footprint; 2) negligible global interconnect on account of the insignificant length of through-silicon vias (TSVs) and furthermore the flexibleness vertical routing, results in advanced execution and diminished power utilization of the interconnects; 3) furthermore of heterogeneous structure: each and every single die can have completely new innovations and collected interconnectivity is considered as the primary advantage in developing execution by contributing the huge data transfer capacity and low-latency TSV structures (Pandiaraj, Sivakumar, & Geetharamani, 2017b). TSV is significant in executing interconnectivity over the layer.
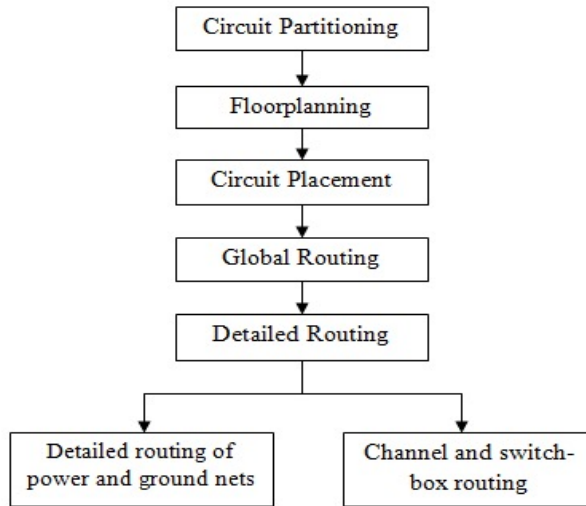
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Figure 1. VLSI Physical Design phases.
Source: own elaboration.

With the improvement in innovation and developing interest for system on a chip (SOC) coordinated circuit had turned out to be increasingly muddled. This makes a major test in IC plan. Among ventures in the outline procedure the routing which is required as the last stride in physical configuration has particularly turned out to be imperative. A better routing will reduce number of interconnections among sub-circuits and result in better routing area of layout (Sivakumar, Pandiaraj, & Prakash, 2019). The main objective of routing includes minimization of wirelength between the modules.

2. MATERIALS AND METHODS

3D GLOBAL ROUTING

The main purpose of a global router is to break down an enormous routing issue into very little and smart sub-issues (detailed routing). This deterioration is done by finding an unpleasant way for every net to remember the final output to reduce the chip size, shorten wire length and uniformly convey the blockage over the routing region. Amid global routing, pins with identical voltage are associated utilizing wire segments. A net is a rendezvous of 2 or additional sticks that have an equivalent potential. within the last chip set up, they need to be associated. A standard p-pin net interfaces one yield stick of a gate

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and p − 1 information pins of different entryways; its fan out resembles p − 1. The term netlist insinuates everything contemplated to all or any nets.

In global routing, the wire parts used by net topologies are no doubt embedded in the chip group. The chip an area is delineated by an unpleasant directing matrix, and available materials are portrayed by edges with specific parameters during a grid graph. Nets are then conveyed to those routing assets. The consequent terms are applicable to global routing by and large.

- A routing way (segment) is accessible there as flat and vertical wiring way. Now and then the net uses a grouping of wavering flat tracks and vertical segments, any place adjoining tracks and sections are associated by between layer vias.

- A routing area could be a locale it ought to contain routing tracks as well as sections.

- The similarly dispersed level and vertical grid lines that produce a standard network over the chip space is making a uniform routing region. This grid is typically referenced as a ggrid (global grid); it's made out of unit gcells (global cells). Grid lines are for the most part dispersed 7 to 40 directing tracks separated to balance out the complexities of the chip-scale global routing and gcell-scale point by point routing issues.

- The horizontal and vertical limits that are adjusted to outer stick associations are making the non-uniform routing region. This coordinates to channels and switchboxes − routing region that have varying sizes. all through global routing, nets are allocated to those directing areas. In detailed routing, every one of the nets are appointed to explicit wiring ways.

- Every one of the pins are situated on the more extended sides of the routing region and there are no pins on the shorter side of the routing region. There are two distinct sorts of channels are accessible - horizontal and vertical.

- A horizontal channel has the pins on the top and base limits of the routing area.

- A vertical channel has the pins on the left and right limits of the routing area.

- The pins of a net are related with the routing channel by segments, which are related with totally various segments by tracks. Because of the developed scope of driving layers in present-day designs, this standard channel model must a decent degree lost its pertinence. Or maybe, over-the-cell (OTC) directing is utilized.

The channel limit is communicated by the quantity of realistic routing tracks or segments. For single-layer routing, the capacity is determined by the tallness h of the channel isolated by the pitch dpitch, any place dpitch is that the base separation between the significant (vertical or even) bearing. For multilayer routing, the capacity(σ) is that the aggregate of the limits all things considered.

$$\sigma(\text{layers}) \;=\; \sum_{\text{layer} \in \text{layers}} [\text{h/dpitch(layer)}]$$

Layers is representing to the arrangement everything being equal, and dpitch (layer) is represents to the directing pitch for the layers.

Objectives and goals of Global routing:

The main aim of global routing is to provide complete information to the detailed router on where to route every interconnection. The objectives of global routing are one or more of the following:

- Total wire length minimization.
- Distribution of congestion over the routing region in an even manner.
- Minimization the critical path delay.
- Probability maximization that the detailed router can complete the routing.

III. THE GLOBAL ROUTING FLOW

A grid graph is illustrated as ggrid = (V, E), any place the nodes v $\in$ V represents the routing framework cells (gcells) and thusly the edges represent to associations of lattice cell sets (vi,vj). the global routing network diagram is two-dimensional, be that as it may, ought to represent to k directing layers. Thus, k unmistakable limits ought to be kept up at each node of the matrix chart. for example, for a two-layer routing network (k = 2), an ability pair (3,1)

for a directing matrix cell will represent to 3 even areas and one vertical section still open. Elective ability portrayals are achievable.

Step 1: Forming the regions of routing area:

In this movement, the design region is detached into routing territories. On occasion, nets will be routed over standard cells (OTC directing). The routing territory units are encircled as 2 Dimensional or 3 Dimensional channels, switch boxes and diverse district types. These different types of routing methodologies are then depicted with a diagram as appeared in Figure 2.
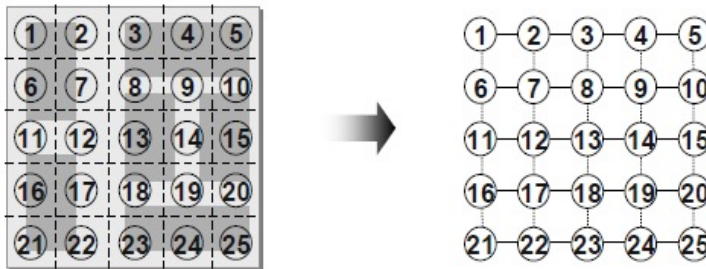

Figure 2. A layout and its corresponding connectivity graph.
Source: own elaboration.

Step 2: Nets are mapping with routing regions:

During this movement, each net of the design is presumably going consigned toward 1 or many routing zones identify with the pins of the routing regions. The routing furthest reaches of each routing area is determined by the quantity of nets crossing the specific locale.

Step 3: Assigning crosspoints:

During movement, also called halfway routing, routes are allocated to adjusted zones or crosspoints. Crosspoint assignment enables scaling of global and detailed routing to traces with a colossal assortment of cells and conjointly disseminated and parallel calculations, since the routing areas will be dealt with self-rulingly in detailed routing. Finding an ideal Crosspoint assignment needs learning of net affiliation conditions and channel requesting. A heuristic for global directing in partner degree network chart has showed up in Figure 3. Connectivity graph for a global routing.

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Input: netlist Netlist, layout LA
Output: routing topologies for each net in Netlist
1. RR = DEFINE_ROUTING_REGIONS(LA)        // define routing regions
2. CG = DEFINE_CONNECTIVITY_GRAPH(RR)      // define connectivity graph
3. nets = NET_ORDERING(Netlist)            // determine net ordering
4. ASSIGN_TRACKS(RR,Netlist)               // assign tracks for all pin
// connections in Netlist
5. for (i = 1 to |nets|)                   // consider each net
6. net = nets[i]
7. FREE_TRACKS(net)                        // free corresponding tracks
// for net's pins
8. snets = SUBNETS(net)                     // decompose net into
                                            // two-pin subnets

9. for (j = 1 to |snets|)
10. snet = snets[j]
11. spath = SHORTEST_PATH(snet,CG)          // find shortest path for snet
                                            // in connectivity graph CG
12. if (spath == Ø)                         // if no shortest path exists,
13. continue                                // do not route
14. else                                    // otherwise, assign snet to
15. ROUTE(snet,spath,CG)                    // the nodes of spath and
                                            // update routing capacities
```

Figure 3. Connectivity graph for a global routing.
Source: own elaboration.

PROBLEM STATEMENT

The routing problem is described as a three-dimensional grid graph. The 3D graph is regenerate into a 2D grid graph to first get the 2D routing result. Lastly, layer assignment is very difficult to assign every net to the corresponding metal layer to get a 3D routing result (Ghosal, Das, & Das, 2012b; Ghosal *et al.*, 2012d). Let pins of a net distributed across n (n≥1) layers of a tool be P= {p1, p2…pn}. Let the set of all nets be N= {n1, n2, …nm}. Let the set of modules be M={m1, m2….mk} contact the routing space, wherever every mi has its coordinates (xi, yi). The wirelength and congestion are determined in line with the algorithm. The difficulty target is to create an entire routing Tree (T) covering the total set (N) utilizing the projected congestion routing strategy. Using this proposed algorithm all the routing regions are resolved with minimum wire-length for all nets. The routing layer are described as a grid structure (Roy & Markov, 2008).

The quality factors which will be employed in global routing to evaluate the standard of the routing result are: i) Wire-length ii) Total overflow.

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IV. PROPOSED ALGORITHM AND RELATED WORK

I. NET DECOMPOSITION:

Multi-pin nets – nets with more than 2 pins – are regularly spoiled into two-pin subnets, trailed by each subnet in venture with certain requests. Such net decay is performed toward the beginning of global routing and may affect the standard of the last routing goals.

II. RECTILINEAR ROUTING:

The rectilinear Steiner Minimal Tree (RSMT) (Sivakumar *et al.*, 2019) and rectilinear Minimum Spanning Tree (RMST) built by utilizing a calculation to decay multi-pin nets into two-pin subnets before routing stages. Be that as it may, the RSMT is mind boggling than RMST as it utilizes the idea of Steiner focuses and is less adaptable than that of RMSTs (Ghosal *et al.*, 2012a). Then again, the RMST creates the blockage mindful routing way of each subnet by utilizing an example or monotonic routing. A heuristic for consecutive Steiner tree is as appeared in Figure 4.

III. RECTILINEAR SPANNING TREE:

All terminals (pins) are associated by a rectilinear Spanning Tree utilizing pin-to-pin associations that are made by vertical and even portions. pin to- pin associations will meet exclusively at a pin, i.e., "crossing" edges don't keep running into, and no further intersections (Steiner focuses) are permitted. The traversing tree isn't delivered if the entire length of fragments is stripped, at that point the tree might be a rectilinear least crossing tree (RMST). Partner RMST is regularly figured in O(p2) time, any place p is that the scope of terminals inside the net utilizing techniques like Prim's calculation (Müller, 2006). This calculation assembles partner mst by starting with one terminal and voraciously adding least-cost edges to the halfway built tree until all terminals are associated. Progressed computational-geometric procedures slice back the runtime to O(p log p).

IV. RECTILINEAR STEINER TREE (RST):

A rectilinear Steiner Tree (RST):

will associate all p pin areas and probably some further areas (Steiner focuses). While any rectilinear spreading over tree for a p-pin net is moreover a rectilinear Steiner tree, the general net length is decreased by including the Steiner focuses. Partner RST could be a rectilinear Steiner least tree (RSMT) if the general length of net portions acclimated interface all p pins is negligible (Roy, Ghosal, & Das, 2014). Fʃor instance, in an exceptionally uniform routing grid, let a unit net stage be a position that interfaces 2 adjoining gcells; partner RST is partner RSMT if it's the base assortment of unit web fragments. The accompanying certainties are recognized with respect to RSMTs. A RSMT for a p-pin net has among 0 and $p - 2$ (comprehensive) Steiner focuses.

- Any routing area pin will have a degree as 1, 2, 3 or 4. A Steiner point has degree either 3 or 4.

- A rectilinear Steiner insignificant Tree is frequently gulped inside the MBB (Minimum Bounding Box) of the net.

- The complete edge length LRSMT of the rectilinear Steiner negligible Tree is at least a large portion of the border of the base-jumping box of the net: LRSMT $\geq$ (LMBB/2).

Building RSMTs inside the general case is NP-hard; practically speaking, heuristic ways are utilized. One brisk philosophy, FLUTE (Chang *et al.*, 2010; Chu & Wong, 2007), discovers ideal RSMTs for up to 9 sticks and creates close insignificant RSTs, typically at interims one hundred forty-five of the base length, for bigger nets. Be that as it may, RSMTs are appropriate for wire length minimization and ill-advised for web topology by and by.

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V. SEQUENTIAL STEINER TREE HEURISTIC:

```
Input: set of all pins P
Output: heuristic Steiner minimum tree T(V,E)
1. P' = P
2. (pA,pB) = CLOSEST_PAIR(P')                        // closest pin pair
3. ADD(V,pA)                                          // add pA to T
4. ADD (V,pB)                                         // add pB to T
5. REMOVE(P',pA)                                      // remove pA from P'
6. REMOVE(P',pB)                                      // remove pB from P'
7. if (P' == Ø)                                       // shortest path connecting
8. ADD(E,L-shape connecting pA and pB)               // pA and pB is any L-shape
9. else
10. curr_MBB = MBB(pA,pB)                             // MBB of pA and pB
11. while (P' || Ø)
12. (pMBB,pC) = CLOSEST_PAIR(curr_MBB,P')  // closest point pair, one from
// curr_MBB, one from P'
13. ADD(V,pMBB)                                       // add pMBB to T
14. ADD(V,pC)                                         // add pC to T
15. REMOVE(P',pC)                                     // remove pC from P'
16. if (pMBB || P)                                    // if pMBB is a pin, either
17. ADD(L-shape connecting pMBB and pC)              // L-shape is shortest path
18. else                                             // if pMBB is not a pin, add
19. ADD(E,L-shape that includes pMBB)                // L-shape that pMBB is on
20. curr_MBB = MBB(pMBB,pC)                           // MBB of pMBB and pC
21. ADD(V,pC)                                         // connect T to remaining pin
22. ADD(E,L-shape connecting pMBB and pC)            // with L-shape
```

Figure 4. Sequential Steiner Tree Heuristic.
Source: own elaboration.

VI. HANAN GRID:

The wire length of the net is diminished by adding Steiner focuses to relate degree RMST. In 1966, Hanan (Dai, Liu, & Li, 2012) prove that to discover a RSMT, it does the trick to consider exclusively Steiner focuses put at the crossing points of vertical and horizontal lines that get together with terminal pins. A lot of officially, the Hanan framework (as appeared in Figure 5) comprises of the lines x = xp, y = yp that get together with each stick area (xp, yp). The Hanan framework contains at the most p2 competitor Steiner focuses, along these lines enormously lessening the territory for finding a best RSMT.
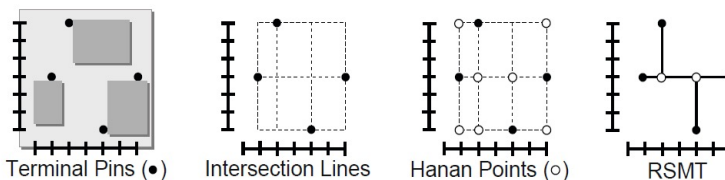

Terminal Pins (●)   Intersection Lines   Hanan Points (○)   RSMT

Figure 5. Getting the Hanan grid and subsequently the Steiner points of an RSMT.
Source: own elaboration.

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VII. RIP-UP AND RE-ROUTE:

In stylish global routing, to maintain a strategic distance from floods, Rip-up and re-routing system especially that depends on exchange strategy are generally utilized that spotlights on expanding the punishment of a network edge to stay away from way watching out on aforesaid flooded framework edges. numerous exchange-based cost capacities are anticipated in (Dai *et al.*, 2012; Liu *et al.*, 2010; Roy *et al.*, 2014). McMurchie and Ebeling (1995) detail the exchange based steering cost work of matrix edges e as pursues:

$$cost(e) = (be + he) \times pe\ldots\ldots\ldots\ldots\ldots (1)$$

where cost(e), be, he, and pe are the cost of routing, the bottom cost, the history cost, and also the congestion penalty of e, severally. As overflow happens the history cost, he will increase.

Also, FGR (Xu, Zhang, & Chu, 2009) formulates another cost perform formula as follows:

$$cost(e) = be + he \times pe\ldots\ldots\ldots\ldots\ldots (2)$$
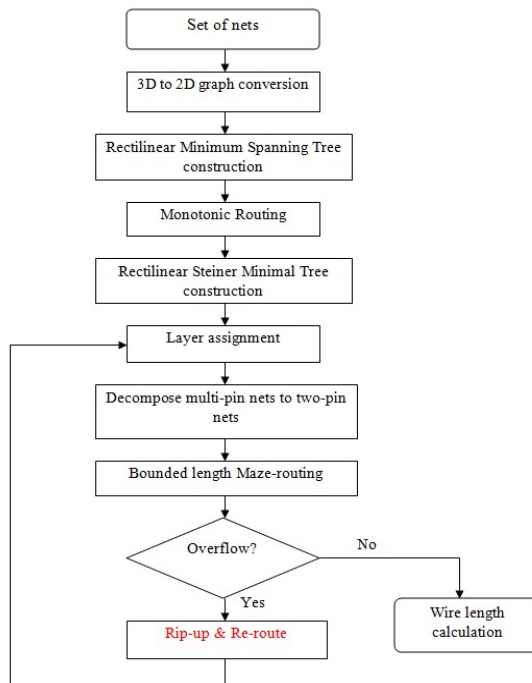

Figure 6. Flow chart for proposed algorithm.
Source: own elaboration.

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VIII. BOUNDED LENGTH MAZE ROUTING:

To reduce the looking through area of maze routing and to quicken maze routing, different global routers will receive a bounding box (Ghosal *et al.*, 2012d) technique and well-ordered loosen up the bounding box if a flood free directing answer can't be found. In any case, maze routing could make a few reroutes or neglect to search out a concise way among the bounding box. Hence, this article creates limited Length Maze Routing (Ghosal *et al.*, 2012d) to accelerate maze routing by lessening the pursuit area comparatively on well improve routing asset usage by change repetitive wirelength. A stream graph for the anticipated recipe is appeared in Figure 6.

IX. WIRELENGTH MINIMIZATION:

The objective of the wire length minimization [19] is so outlined as follows:

The trivial edge on the number of tracks is larger than the peak of a particular vertex vi (corresponding to net ni) in vct i. e.

Max (dtmax, vtmax)>htvi

Then we are able to prorogue the present assignment of ni wherever dmax= channel density, VC= (V, A) is built to represent the vertical constraints h= height of the vertex. wherever tvi= chosen vertex.

3. RESULTS

The proposed algorithms were implemented in C/C++ language. ISPD 2007 (Nam, 2007) and ISPD 2008 (Sze, 2008) benchmark circuits were employed in our experiments. The wirelength is in small units and therefore the overflow altogether cases are zero. The results were compared with NCTU-GR (Chang, Lee, & Wang, 2008) and NTHU-GR (McMurchie & Ebeling, 1995; Liu *et al.*, 2013).

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Table 1. Comparison of wire lengths of planned global router with NCTU-GR and NTHU-GR on overflow free cases.

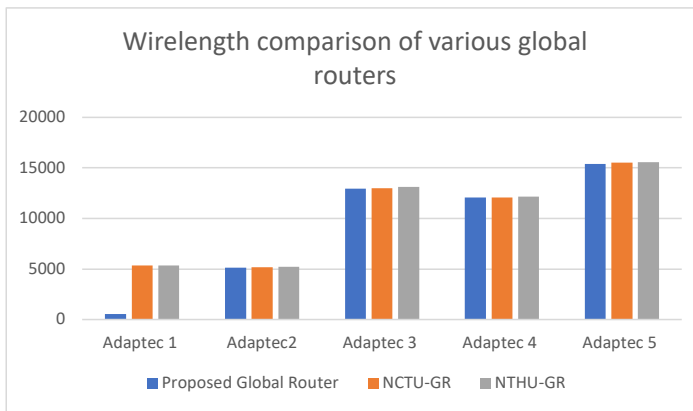| Comparison of wirelength (in micro units) of various global routers with the Planned Global router			
Benchmark	Proposed Global Router	NCTU-GR	NTHU-GR
Adaptec 1	5304K	5350K	5349K
Adaptec 2	5151K	5197K	5230K
Adaptec 3	12924K	13008K	13111K
Adaptec 4	12053K	12062K	12172K
Adaptec 5	15401K	15501K	15555K

Source: own elaboration.

Figure 7. Results.
Source: own elaboration.

The Figure 7 provided here shows the Wire-length results on the ISPD2008 benchmarks. The test problem varies from adaptec1 to adaptec5. The proposed global router is compared with the existing techniques.

4. CONCLUSIONS AND FUTURE WORK

This work presents a novel global routing scheme by using RSMT and RSMT algorithms for net decomposition, monotonic routing for routing all the nets, bounded length maze routing to find the shortest paths for wire length minimization. Negotiation primarily based rip-up and re-routing theme is employed to avoid the congestion. Congestion is represented in terms of overflow. If overflow occurs the nets are ripped-up and re-routed by redefining

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the layers, decomposing the multi-pin nets and then bounded length maze routing is applied again and this process is repeated until the overflow is zero. In future using machine learning methodology the temperature has been reduced between the layers.

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REFERENCES

Chang, Y.-J., Lee, T.-H., & Wang, T.-C. (2010). GLADE: A modern global router considering layer directives. In *2010 IEEE/ACM International Conference on Computer-Aided Design (ICCAD)*, 319–323. https://doi.org/10.1109/ICCAD.2010.5654094

Chang, Y.-J., Lee, Y.-T., & Wang, T.-C. (2008). NTHU-route 2.0: A fast and stable global router. In *2008 IEEE/ACM International Conference on Computer-Aided Design,* pp. 338–343.2008. https://doi.org/10.1109/ICCAD.2008.4681595

Chen, H.-Y., Hsu, C.-H., & Chang, Y.-W. (2009). High-performance global routing with fast overflow reduction. In *2009 Asia and South Pacific Design Automation Conference,* pp. 582–587. https://doi.org/10.1109/ASPDAC.2009.4796543

Chu, C., & Wong, Y.-C. (2007). FLUTE: Fast Lookup Table Based Rectilinear Steiner Minimal Tree Algorithm for VLSI Design. *IEEE Transactions On Computer-Aided Design, 27*(1), 70-83. https://doi.org/10.1109/TCAD.2007.907068

Dai, K.-R., Liu, W.-H., & Li, Y.-L. (2012). NCTU-GR: Efficient simulated evolution-based rerouting and congestion-relaxed layer assignment on 3-D global routing. *IEEE TVLSI, 20*(3), 459–472. https://doi.org/10.1109/TVLSI.2010.2102780

3C Tecnología. Glosas de innovación aplicadas a la pyme. ISSN: 2254 – 4143

Edición Especial Special Issue
Noviembre 2021

Ghosal, P., Das, A., & Das, S. (2012a). Obstacle Aware RMST Generation Using Non-Manhattan Routing for 3D ICs. *ACITY,* (3), 657–666. https://doi.org/10.1007/978-3-642-31600-5_64

Ghosal, P., Das, S., & Das, A. (2012b). A Novel Algorithm for Obstacle Aware RMST Construction during Routing in 3D ICs. *ACITY,* (2), 649–658. https://doi.org/10.1007/978-3-642-31552-7_65

Ghosal, P., Das, S., & Das, A. (2012c). A New Class of Obstacle Aware Steiner Routing in 3D Integrated Circuits. *ACITY,* (3), 697–706. https://doi.org/10.1007/978-3-642-31600-5_68

Ghosal, P., Rahaman, H., Das, S., Das, A., & Dasgupta, P. (2012d). Obstacle Aware Routing in 3D Integrated Circuits. In Thilagam, P. S., Pais, A. R., Chandrasekaran, K., & Balakrishnan, N. (eds.) *Advanced Computing, Networking and Security.* ADCONS 2011. Lecture Notes in Computer Science, vol. 7135. Springer, Berlin, Heidelberg. https://doi.org/10.1007/978-3-642-29280-4_53

Goplen, B., & Sapatnekar, S. (2005). Thermal Via Placement in 3D ICs. In *Proceedings of the International Symposium on Physical Design,* pp. 167–174. https://doi.org/10.1145/1055137.1055171

Kahng, A. B., Lienig, J., Markov, I. L., & Hu, J. (2011). *VLSI Physical Design_ From Graph Partitioning to Timing Closure.* Springer. https://doi.org/10.1007/978-90-481-9591-6

Liu, W.-H., Kao, W.-C., Li, Y.-L., & Chao, K.-Y. (2010). Multi-threaded collision-aware global routing with bounded-length maze routing. In *Proceedings of the 47th Design Automation Conference (DAC),* pp. 200–205. https://doi.org/10.1145/1837274.1837324

Liu, W.-H., Kao, W.-C., Li, Y.-L., & Chao, K.-Y. (2010). Multi-Threaded Collision-Aware Global Routing with Bounded-Length Maze Routing. In *Proceedings of Design Automation Conference (DAC),* pp. 200-205. https://doi.org/10.1145/1837274.1837324

Liu, W.-H., Kao, W.-C., Li, Y.-L., & Chao, K.-Y. (2013). NCTU-GR 2.0: Multithreaded Collision-Aware Global Routing with Bounded-Length Maze Routing. *IEEE*

3C Tecnología. Glosas de innovación aplicadas a la pyme. ISSN: 2254 – 4143

Edición Especial Special Issue
Noviembre 2021

Transactions On Computer-Aided Design Of Integrated Circuits And Systems, 32(5), 709-722. https://doi.org/10.1109/TCAD.2012.2235124

McMurchie, L., & Ebeling, C. (1995). Pathfinder: A negotiation-based performance-driven router for FPGAs. In *3rd International ACM Symposium on Field-Programmable Gate Arrays,* pp. 111−117. https://doi.org/10.1109/FPGA.1995.242049

Minz, J., Wong, E., & Lim, S. K. (2005). Thermal and Crosstalk-Aware Physical Design for 3D System-On-Package. In *Proceedings of Electronic Components and Technology Conference,* pp. 824−831. https://doi.org/10.1109/ECTC.2005.1441368

Müller, D. (2006). Optimizing yield in global routing. In *2006 IEEE/ACM International Conference on Computer Aided Design,* pp. 480−486. https://doi.org/10.1109/ICCAD.2006.320161

Nam, G.-J. (2007). *ISPD 2007 Contest.* http://archive.sigda.org/ispd2007/contest.html

Ozdal, M. M., & Wong., M. D. F. (2007). ARCHER: A history-driven global routing algorithm. In *2007 IEEE/ACM International Conference on Computer-Aided Design*, pp. 488−495. https://doi.org/10.1109/ICCAD.2007.4397312

Pandiaraj, K., Sivakumar, P., & Geetharamani, N. (2017b). Reduction of temperature rise in 3D IC routing. In *2017 IEEE International Conference on Electrical, Instrumentation and Communication Engineering (ICEICE)*, pp. 1-5. https://doi.org/10.1109/ICEICE.2017.8191907

Pandiaraj, K., Sivakumar, P., & Sridevi, R. (2017a). Minimization of wirelength in 3d IC routing by using differential evolution algorithm. In *2017 IEEE International Conference on Electrical, Instrumentation and Communication Engineering (ICEICE)*, pp. 1-5. https://doi.org/10.1109/ICEICE.2017.8191950

Roy, D., Ghosal, P., & Das, N. (2014). A Thermal and Congestion Driven Global Router For 3D Integrated Circuits. *Proceeding of the 2014 IEEE Students' Technology Symposium*, pp. 303-308. https://doi.org/10.1109/TechSym.2014.6808065

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Roy, D., Ghosal, P., & Das, N. (2014). A Thermal And Congestion Driven Global Router For 3D integrated Circuits. *Proceedings of the 2014 IEEE Students' Technology Symposium,* pp. 303-308. https://doi.org/10.1109/TechSym.2014.6808065

Roy, J. A., & Markov, I. L. (2008). High-performance routing at the nanometer scale. *IEEE TCAD, 27*(6), 1066–1077. https://doi.org/10.1109/TCAD.2008.923255

Sivakumar, P., Pandiaraj, K., & Prakash, K. J. (2019). Optimization of Thermal Aware Multilevel Routing For 3D IC. *International journal of analog integrated circuits and signal processing, 103*(1), 131-142. https://doi.org/10.1007/s10470-019-01513-y

Sze, C. (2008). ISPD 2008 *Contest.* http://archive.sigda.org/ispd2008/contests/ispd08rc.html

Xu, Y., & Chu, C. (2011). MGR: Multi-level global router. In *2011 IEEE/ACM International Conference on Computer-Aided Design (ICCAD),* pp. 250–255. https://doi.org/10.1109/ICCAD.2011.6105336

Xu, Y., Zhang, Y., & Chu, C. (2009). FastRoute 4.0: Global router with efficient via minimization. In *2009 Asia and South Pacific Design Automation Conference,* pp. 576–581. https://doi.org/10.1109/ASPDAC.2009.4796542