DISCONTINUOUS CONDUCTION MODE BUCK CONVERTER WITH HIGH EFFICIENCY

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ABSTRACT

Electronic devices require AC to DC converter (rectifier) to convert AC voltage from the grid to DC voltage for the electronics and its result is low power factor (PF) and harmonic current injection into the system. Nowadays, power factor correction (PFC) converters are being widely used which can achieve high power factor (PF) and reduce the harmonics caused during AC to DC conversion and buck PFC converter is one of mostly used converter. On the other hand, if this converter works with constant duty-cycle (CDC) control scheme, the overall losses are more and efficiency is less. In order to increase the efficiency of buck converter operating in discontinuous conduction mode (DCM), a variable duty-cycle (VDC) control scheme is proposed. The method of fitting VDC control scheme is given for making implementation of circuit simpler. The performance of buck converter is compared with CDC and VDC control scheme in terms of efficiency. For verifying the validity of proposed technique, the simulation results are carried out. The object of the research paper is to propose the control scheme to achieve high PF for DCM buck converter by only modulating the duty-cycle of buck switch.

KEYWORDS

Variable Duty-Cycle (VDC), Constant Duty-Cycle (CDC), Discontinuous Conduction Mode (DCM), Electromagnetic Interference (EMI), Duty-Cycle, Buck Converter.

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1. INTRODUCTION

Electronic devices require AC to DC converter (rectifier) to convert AC voltage from the grid to DC voltage for the electronics and its result is low power factor (PF) and harmonic current injection into the system. Nowadays, power factor correction (PFC) converters are being widely used which can achieve high power factor (PF) and reduce the harmonics caused during AC to DC conversion (Praneeth & Williamson, 2018; Williamson, Rathore & Musavi, 2015; Nussbaumer *et al.*, 2019; Anwar *et al.*, 2017; Al Gabri, Fardoun & Ismail, 2015; Badawy, Sozer & De Abreu-Garcia, 2016; Memon *et al.*, 2019a, 2019b, 2019c, 2019d, 2019e).

Power factor correction can be of two types: active PFC and passive PFC. Active PFC can be achieved by using passive elements like inductors, capacitors and inductors and passive PFC can be achieved by using electronic circuits with active switches like insulated gate bipolar junction transistor (IGBT) and metal oxide semiconductor field effect transistor (MOSFET), etc. To obtain the good value of power factor and meet the standards like IEC61000-3-2 and IEEE 519, active power factor correction (PFC) techniques are used. DC to DC converters used as power factor correction circuits with the help of active switches shape the value of supply current which not only improves the PF, but also reduce the harmonics. Among DC-DC converters, DCM buck PFC is generally utilized in many applications because of various advantages like maintaining high efficiency for the wide range of input voltage, cost reduction, low output voltage, protection against inrush current life time improvement and easy design of electromagnetic interference (EMI) filter The major drawback of the buck converter is its PF is low and efficiency is also low, especially when operated with constant duty-cycle control scheme (CDCCS).

For modifying the performance of traditional buck converter, various research has proposed various topologies and control schemes (Endo, Yamashita & Sugiura, 1992; Lee, Wang & Hui, 1997; Spiazzi & Buso, 2000; Huber, Gang & Jovanovic, 2011; Jang & Jovanović, 2011; Lamar *et al.*, 2012; Ki & Lu, 2013; Al Gabri, Fardoun & Ismail, 2015; Memon *et al.*, 2016; Memon *et al.*, 2017; Memon *et al.*, 2018a, 2018b; Memon *et al.*, 2019a, 2019b, 2019c, 2019d, 2019e; Liu *et al.*, 2020).

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Most of the work in the literature is done to improve the PF of the buck converter. The purpose of this paper is to introduce the control scheme which can improve the efficiency of DCM buck converter.

In this paper, a variable duty-cycle control scheme (VDCCS) is introduced for DCM buck converter to reduce peak and rms current of inductor and hence ultimately enhancing its efficiency.

This paper is divided into six sections. In section 2, the operation states of DCM buck converter are analyzed with traditional CDCCS strategy. The introduced VDCCS is discussed in section 3. Then the comparative analysis is discussed in section 4 in terms of efficiency. In section 5, the effectiveness of proposed topology is evaluated by simulation results. Finally, some conclusions are drawn in section 6.

2. RESEARCH METHODOLOGY

The research methodology is based on:

1. Mathematical analysis of the operating principle of the control schemes for DCM Buck converter with the help of MATHCAD converter.
2. Introducing the proposed control scheme to obtain high efficiency
3. Realization of control scheme through control blocks.
4. Comparative analysis of the converter for CDCC and VDCC strategy
5. Developing the simulation model of DCM Buck converter with the help of MATLAB software
6. Confirming the results.

3. CONVENTIONAL CDC CONTROL SCHEME FOR BUCK CONVERTER

Figure 1(b) shows the main circuit of a buck converter with CDC control scheme.

The input voltage before and after the bridge are given as

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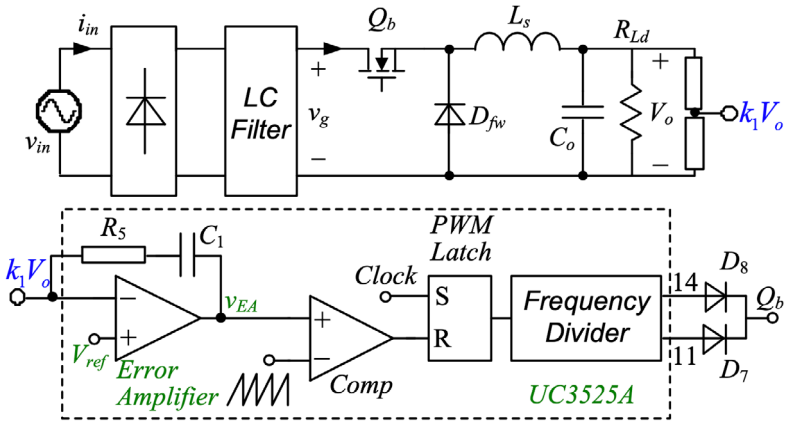

Figure 1. Buck converter with CDC control scheme.
Source: (Yao *et al.*, 2017).

$$v_{in}(\theta) = v_g = \sqrt{2}V_{rms}\sin\theta \tag{1}$$

Where V_{rms} is the rms value.

There are three switching cycles when buck converter works in discontinuous conduction mode (DCM).

When Q_b conducts, the inductor is getting charge from supply voltage in first switching cycle as depicted in Figure 2.

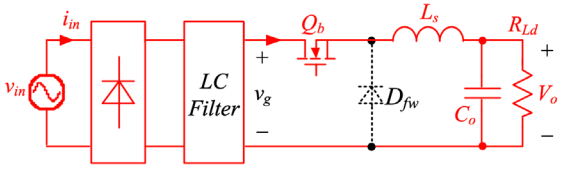

Figure 2. Buck converter during first switching cycle.
Source: (Yao *et al.*, 2017).

The peak current of inductor i_{L_pk} is given as

$$i_{L\_pk} = \frac{\sqrt{2}V_{rms}\sin\theta - V_o}{L_s} D_{on}T_s \tag{2}$$

Where D_{on} is the duty-cycle of during turn on time of switch

When Q_b is off, inductor is discharging through load and output capacitor, as shown in in Figure 3. It occurs in second switching cycle

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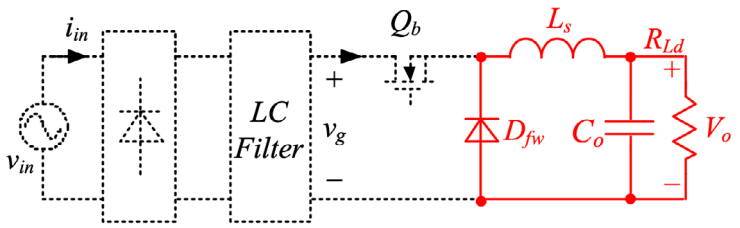

Figure 3. Buck converter during second switching cycle.
Source: (Yao *et al.*, 2017).

The peak current of inductor i_{L_pk} is

$$i_{L\_pk} = -\frac{V_o}{L_s} D_{on} T_s \tag{3}$$

By using the information of volt-second balance, following expression is obtained

$$(\sqrt{2} V_{rms} \sin\theta - V_o) D_{on} T_s = V_o D_{off} T_s \tag{4}$$

From (2) and (4), the following relation is obtained

$$D_{off} = \frac{\sqrt{2} V_{rms} \sin\theta - V_o}{V_o} D_{on} \tag{5}$$

During third switching cycle, output capacitor is discharged through load as shown in Figure 4.

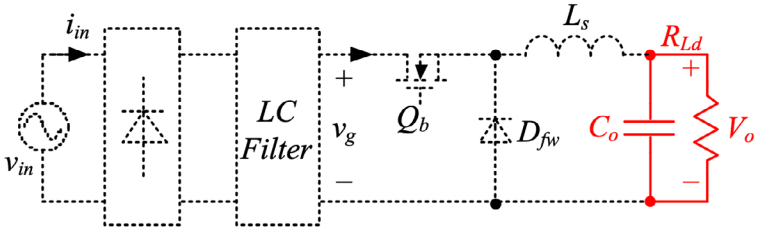

Figure 4. Buck converter during third switching cycle.
Source: (Yao *et al.*, 2017).

The value of average input current for buck converter is got as

$$i_{b\_av\_cdccs} = \frac{D_{on}^2 (\sqrt{2} V_{rms} \sin\theta - V_o)}{2 L_s f_s} \tag{6}$$

For complete half cycle, input current is expressed as

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$$i_{in\_b\_cdccs} = \begin{cases} \frac{D_{on}{}^2(\sqrt{2}V_{rms}\sin\theta - V_o)}{2L_s f_s} & \theta_0 < \theta < \pi - \theta_0 \\ 0 & 0 \le \theta < \theta_0 \;\&\; \pi - \theta_0 < \theta \le \pi \end{cases}$$

$$\text{Where } \theta_0 = \arcsin V_o / \text{sqrt } 2 * V_{rms} \tag{7}$$

Based on (1) and (7), the input power of the buck converter is expressed as

$$P_{in\_cdccs} = \frac{\sqrt{2}V_{rms}D_{on}^2}{2\pi L_s f_s}\int_{\theta_0}^{\pi-\theta_o}\sin\theta(\sqrt{2}V_{rms}\sin\theta - V_o)d\theta \tag{8}$$

Now D_{on} can be calculated by assuming the efficiency of buck converter as 100%

$$D_{on} = \sqrt{\frac{2\pi L_s f_s P_o}{\sqrt{2}V_{rms}\int_{\theta_0}^{\pi-\theta_o}\sin\theta(\sqrt{2}V_{rms}\sin\theta - V_o)d\theta}} \tag{9}$$

4. PROPOSED VDC CONTROL SCHEME FOR BUCK CONVERTER FOR EFFICIENCY IMPROVEMENT

4.1. VDC CONTROL SCHEME FOR EFFICIENCY IMPROVEMENT

For obtaining, high efficiency, the variation rule for duty-cycle must be

$$D_{on\_vdccs} = \sqrt{\frac{D_c V_m \sin\theta}{\sqrt{2}V_{rms}\sin\theta - V_o}} \tag{10}$$

Where Dc is a co-efficient,

By substituting the value of D_{on} in (6), we obtain

$$i_{in\_b\_vdccs} = \frac{\sqrt{2}V_{rms}\sin\theta D_c T_s}{2L_s} \tag{11}$$

The average value of input power with VDC control scheme is expressed as

$$P_{in\_b\_vdccs} = \frac{1}{\pi}\int_{\theta_0}^{\pi-\theta_0}\frac{D_c T_s\left(\sqrt{2}V_{rms}\sin\theta\right)^2}{2L_s}d\theta = P_o \tag{12}$$

The value of D_c is got from (12) as

$$D_c = \frac{4\pi L_s P_o}{\left(\sqrt{2}V_{rms}\right)^2(\pi - 2\theta_0 + \sin 2\theta_0)T_s} \tag{13}$$

By substituting the value of D_c in (11), we get

$$D_{on\_vdccs} = \sqrt{\frac{4\pi P_o L_s \sin\theta}{(\pi - 2\theta_0 + \sin 2\theta_0)\left(\sqrt{2}V_{rms}\sin\theta - V_o\right)\sqrt{2}\,\mathrm{V}_{rms}T_s}} \tag{14}$$

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4.2. FITTING VDC CONTROL SCHEME

For the implementation of Don_vdccs, it is essential to remove squire root term from (14). Because it is difficult to realize to it by using analogue circuits.

Defining $a=V_m/V_o$, $y=sin\theta$, eq. (14) can be simplified as

$$D_{on\_fit} = D_1\left(1-\frac{y}{2ay_0^{\,2}-y_0}\right)$$

$$\text{where } D_1 = \sqrt{\frac{D_0 a y_0}{a y_0 - 1}}\,\frac{2ay_0-1}{2(ay_0-1)}. \tag{15}$$

$y_0=0.75$

Eq. 15 can be rewritten as

$$D_{on\_fit} = D_1\frac{1.125V_m - 0.75V_o - V_o\sin\theta}{1.125V_m - 0.75V_o} \tag{16}$$

The average input current with VDCCS is given as

$$i_{b\_VDCCS} = \frac{(\sqrt{2}V_{rms}\sin\theta - V_o)}{2L_s f_s} D_{on\_fit}^{\,2} \tag{17}$$

5. EFFICIENCY COMPARISON

5.1. LOSS DUE TO BRIDGE DIODE RECTIFIER

The loss caused by bridge diode rectifier is calculated as below

$$P_{con\_bridge(cdccs)} = 2V_{FD}I_{in\_avg(cdccs)} \tag{18(a)}$$

$$P_{con\_bridge(vdccs)} = 2V_{FD}I_{in\_avg(vdccs)} \tag{18(b)}$$

KBL10 is adopted as the rectifier bridge, whose forward voltage drop VFD is 0.9 V.

The input current with CDC control scheme and VDC control scheme is given as

$$i_{b\_cdccs} = \frac{2\pi L_s f_s P_o(\sqrt{2}V_{rms}\sin\theta - V_o)}{2\sqrt{2}L_s f_s V_{rms}\int_{\theta_0}^{\pi-\theta_0}\sin\theta(\sqrt{2}V_{rms}\sin\theta - V_o)d\theta} \tag{19(a)}$$

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$$i_{b\_vdccs} = \frac{\left(D_1 \sqrt{\frac{D_0 a y_0}{a y_0 - 1}} \frac{2 a y_0 - 1}{2(a y_0 - 1)} \frac{1.125 V_m - 0.75 V_o - V_o \sin\theta}{1.125 V_m - 0.75 V_o} \right)^2 (\sqrt{2} V_{rms} \sin\theta - V_o)}{2 L_s f_s} \quad (19(b))$$

5.2. CONDUCTION LOSSES OF THE SWITCHES

The rms current of the on time period, i.e., the rms current of switch Q_b can be got as

$$I_{rms(Qb\_on)} = \sqrt{\frac{\int_{\theta_0}^{\pi-\theta_0} i_{L\_pk}^2 D_{on}\, d\theta}{3\pi}} \quad (20)$$

The rms current of the off time period can be determined as

$$I_{rms(Qb\_off)} = \sqrt{\frac{\int_{\theta_0}^{\pi-\theta_0} i_{L\_pk}^2 D_{off}\, d\theta}{3\pi}} \quad (21)$$

While Q_b is on and off, the current flows through the winding of the inductor, whose rms current is

$$I_{rms(cdccs)} = \sqrt{I_{rms(Qb\_on\_cdccs)}^2 + I_{rms(Qb\_off\_cdccs)}^2} \quad (22(a))$$

$$I_{rms(vdccs)} = \sqrt{I_{rms(Qb\_on\_vdccs)}^2 + I_{rms(Qb\_off\_vdccs)}^2} \quad (22(b))$$

The losses due to conduction of switches can be got as

$$P_{con\_switches(cdccs)} = I_{rms(Qb\_on\_cdccs)}^2 R_{DS(on)\_S} \quad (23(a))$$

$$P_{con\_switches(vdccs)} = I_{rms(Qb\_on\_vdccs)}^2 R_{DS(on)\_S} \quad (23(b))$$

The value of $R_{DS(On)}$ 0.19 Ω which is found from datasheet of 20N60C3.

5.3. LOSSES DUE TURN OFF SWITCHES

The loss caused by turning off the switch with CDC control scheme and VDC control scheme is calculated as

$$P_{off\_switches(cdccs)} = \frac{T_s t_f}{2\pi} \int_0^{\pi} i_{L\_pk\_cdccs} (V_m \sin\theta) d\theta \quad (24(a))$$

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$$P_{off\_switches(vdccs)} = \frac{T_s t_f}{2\pi} \int_0^{\pi} i_{L\_pk\_vdccs} \left(V_m \sin\theta\right) d\theta \tag{24(b)}$$

Where t_f value is 12ns for CMOS 20N60C.

5.4. THE LOSS CAUSED BY COPPER OF THE INDUCTOR

The inductor's copper loss with CDCCS and VDCCS can be found below as

$$P_{copper(cdccs)} = I^2_{rms(cdccs)Lf} R_{copper(Lf)} + I^2_{rms(cdccs)Hf} R_{copper(Hf)} \tag{25(a)}$$

$$P_{copper(vdccs)} = I^2_{rms(vdccs)Lf} R_{copper(Lf)} + I^2_{rms(vdccs)Hf} R_{copper(Hf)} \tag{25(b)}$$

Where $R_{copper(Lf)}$ is 0.16 and $R_{copper(Hf)}$ is 0.23.

The low frequency and high frequency of rms current can be found out by using below formula

$$I_{rms\_lf} = \sqrt{\frac{1}{\pi}\int_0^{\pi} i^2_{L\_ave} d\theta} = \sqrt{\frac{1}{\pi}\int_0^{\pi} \left[\frac{D_y^2 T_s v_g \left(v_g - V_o\right)}{2L_b V_o}\right]^2 d\theta} \tag{26(a)}$$

$$i_{rms\_hf} = \sqrt{\frac{1}{T_s}\int_0^{T_s} (i_L(t) - i_{L\_ave})^2 dt} \tag{26(b)}$$

$$I_{rms\_hf} = \sqrt{\frac{1}{\pi}\int_0^{\pi} i^2_{rms\_hf} d\theta} \tag{26(c)}$$

5.5. LOSS DUE TO CORE OF THE INDUCTOR

The loss caused by core of inductor with CDCCS and VDCCS is calculated as

$$P_{core(cdccs)} = \left[\int_0^{\pi} C_m f_{s(cdccs)}{}^x B_{ac(cdccs)}{}^y \left(ct_0 - ct_1 T_a - ct_2 T_a^2\right) d\theta\right] \frac{10^3 V_e}{\pi} \tag{27(a)}$$

$$B_{ac(cdccs)} = \frac{L i_{L\_pk\_cdccs}}{2NA_e} \tag{27(b)}$$

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$$P_{core(vdccs)} = \left[\int_0^{\pi} C_m f_{s(vdccs)}{}^{x} B_{ac(vdccs)}{}^{y} \left(ct_0 - ct_1 T_a - ct_2 T_a^2\right) d\theta\right] \frac{10^3 V_e}{\pi} \quad (27(c))$$

$$B_{ac(vdccs)} = \frac{Li_{L\_pk\_vdccs}}{2NA_e} \quad (27(d))$$

The value of core parameters can be found from [24].

5.6. THE LOSS DUE TO CONDUCTION OF THE FREEWHEELING DIODE

The conduction loss due to freewheeling diode with CDC and VDC control scheme is

$$P_{con\_freewheelingdiode(cdccs)} = \frac{V_{FD_{fw}}}{\pi} \int_0^{\pi} \frac{i_{pk(cdccs)}}{2} D_{off}\, d\theta \quad (28(a))$$

$$P_{con\_freewheelingdiode(vdccs)} = \frac{V_{FD_{fw}}}{\pi} \int_0^{\pi} \frac{i_{pk(vdccs)}}{2} D_{off}\, d\theta \quad (28(b))$$

The value of VFD is 0.67 for MUR 860 diode.

5.7. THE EFFICIENCY COMPARISON

The efficiency of DCM buck converter with CDC and VDC control scheme can be calculated as

$$\eta_{(cdccs)} = \frac{P_o}{\left[\begin{array}{l} P_o + P_{con\_bridge(cdccs)} + P_{con\_switches(cdccs)} + P_{off\_switches(cdccs)} \\ + P_{copper(cdccs)} + P_{core(cdccs)} + P_{con\_freewheelingdiode(cdccs)} \end{array}\right]} \quad (29(a))$$

$$\eta_{(vdccs)} = \frac{P_o}{\left[\begin{array}{l} P_o + P_{con\_bridge(vdccs)} + P_{con\_switches(vdccs)} + P_{off\_switches(vdccs)} \\ + P_{copper(vdccs)} + P_{core(vdccs)} + P_{con\_freewheelingdiode(vdccs)} \end{array}\right]} \quad (29(b))$$

From above equations and parameters of converter, the theoretical efficiency of converter with CDC and VDC control scheme is calculated and compared as shown in Figure 5. It can be concluded that efficiency of DCM buck converter has improved in case of VDC control scheme.

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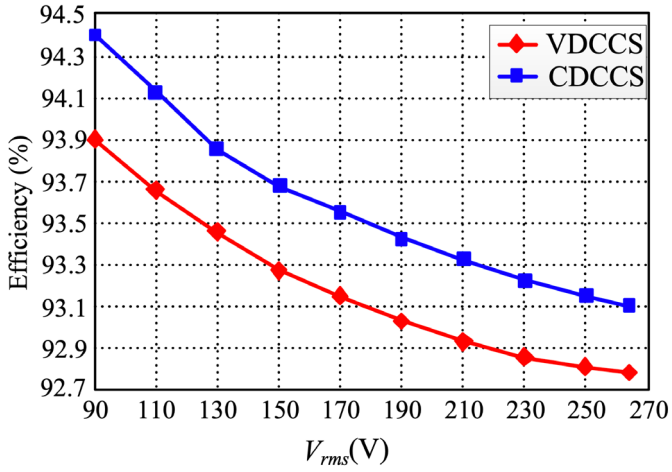

Figure 5. Efficiency at universal input voltage. Mathcad eq: (16-29).

6. SIMULATION RESULTS

For verifying the effectiveness of VDCCS strategy, simulations are carried out. The input voltage range is 90-264VAC, and the output is 80V. For ensuring the current to be in DCM, UC3525A IC is used. All the components in the circuit are selected as idea.

Figure 6 and Figure 7 show the simulation waveforms of input voltage, input current and output voltage of DCM buck converter with CDCCS and VDCCS at 220VAC inputs, respectively. It can be seen that the input current with VDCCS has less peaks as compared to input current with CDCCS is more sinusoidal as compared with CDCC.

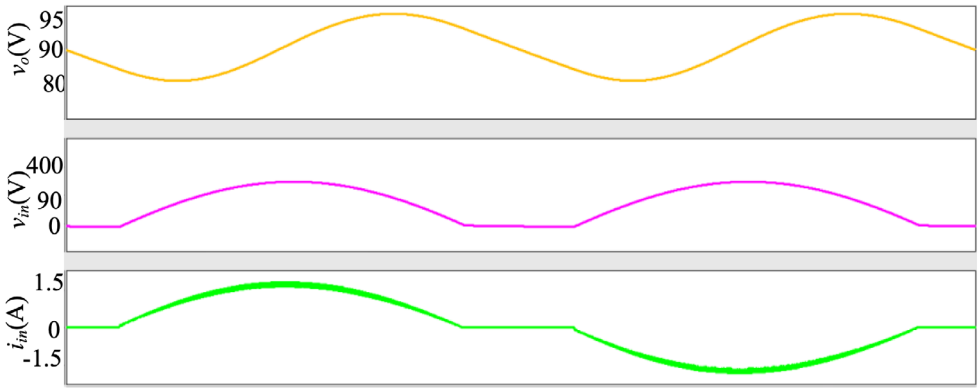

Figure 6. v_o, and v_{in}, i_{in} with CDC control scheme [Simulation waveform from Saber Software].

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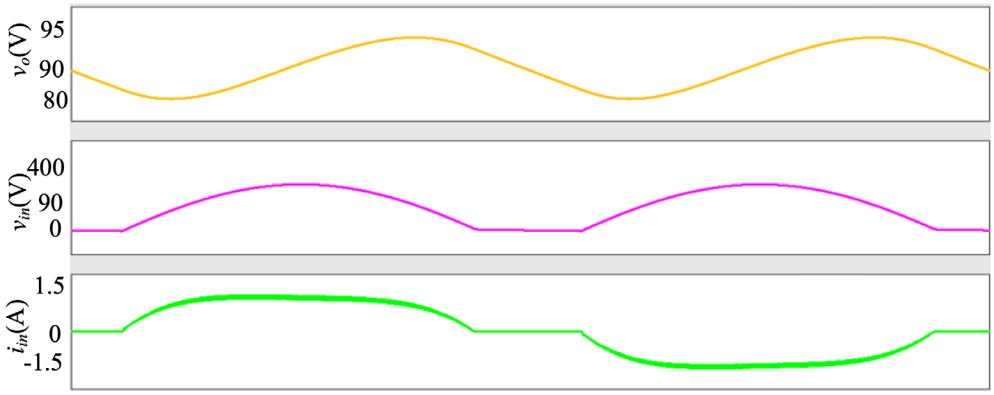

Figure 7. v_o, and v_{in}, i_{in} with VDC control scheme [Simulation waveform from Saber Software].

7. CONCLUSIONS

Electronic devices require AC to DC converter (rectifier) to convert AC voltage from the grid to DC voltage for the electronics and its result is low power factor (PF) and harmonic current injection into the system. Nowadays, power factor correction (PFC) converters are being widely used which can achieve high power factor (PF) and reduce the harmonics caused during AC to DC conversion and discontinuous conduction mode (DCM) buck PFC converter is one of mostly used converter. The DCM buck converter is generally utilized in many applications because of various advantages like maintaining high efficiency for the wide range of input voltage, cost reduction, low output voltage, protection against inrush current and life time improvement. However, its efficiency is low when operated with constant duty-cycle control scheme. For increasing the efficiency and ultimately reducing the losses of the DCM buck converter, a variable duty-cycle control scheme has been introduced. Fitting duty-cycle method is also discussed to make circuit implementation easier. For verifying the validity of proposed technique, the simulation results are carried out.

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