DESIGN AND OPTIMIZATION OF REVERSIBLE LOOK AHEAD CARRY ADDER AND CARRY SAVE ADDER

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ABSTRACT

A circuit is said to be reversible if inputs and the outputs are equal. Reversibility focused mainly to bring down power to zero. In modern centuries, gates with reversible logic has arose together as notable vital approaches for power optimisation based on application. Reversible logic is leading area in power consumption. Based on its application, its emerging trend in power consumption. In ideal situations, reversible circuit yield nil power. In this paper, new design of the look ahead carry adder and carry save adder designed and it is optimized with the previous existing binary logic gates. Minimizing the garbage output and replacing the binary logic gates by reversible logic gates. To develop low power circuits, reversible circuit is necessary.

KEYWORDS

Look ahead carry adder, Carry save adder, Reversible logic.

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1. INTRODUCTION

Look ahead carry adder is a type of digital adder. In this circuit, speed can be increased by reducing the required time. Generated carry bit calculated before summing so that it can reduce the time delay. The design of ripple carry circuit is modest, but it has time-consuming delay in the circuit due to several gates in path carry flows from LSB to MSB. Therefore, in this paper designed an alternate design, *look ahead carry adder*. For designing look ahead carry adder, transform ripple carry design to strategy, which reduce the number of bits to two level bit logic.

By using carry-save adder design sum up multiple binary numbers**.** When compared to other adder design, carry look ahead adder design be at variance in dualistic outputs that has same aspect as inputs, first output has been series of half done sum and next output has been series of carry.

A. NEED FOR REVERSIBLE LOGIC

Reversible circuits are effectual than irreversible because of information loss which leads to energy loss. Due to information loss in irreversibility, it dissipates more power. To reduce power, circuit designed with reversible logic. At last, reversible circuits can be viewed as distinct instance of quantum circuits since quantum progression must be reversible.

B. CONDITIONS FOR REVERSIBLE COMPUTATION

Reversible computation satisfies the conditions.

The foremost State:

Formost state is logical reversibility in which any settled device to be reversible state and the input and output should be unambiguously recoverable from one another.

The second State:

The second state is physical reversibility, the device in reality run backwards, i.e., each operation converts no energy to heat and produces no entropy.

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Representation of a reversible circuit truth table

In view of the fact that we are dealing only with bijective functions, i.e., permutations, we signify them using the pedal system which represented by dislodge cycle of functions.

S_n, denoted as set of all permutations of n indices and S_2^n mentioned as set of objective perform with n input binary bits. Let us Toffoli's Gate and its corresponding truth table.

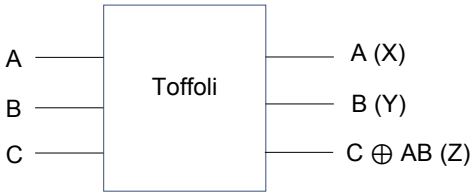

Figure 1. Toffoli gate.

Table 1. Truth table for toffoli gate.

Inputs			Outputs		
A	B	C	X	y	Z
0	0	0	0	0	0
0	0	1	0	0	1
0	1	0	0	1	0
0	1	1	0	1	1
1	0	0	1	0	0
1	0	1	1	0	1
1	1	0	1	1	1
1	1	1	1	1	0

Some special types of Reversible Gates

SWAP Gate:

Reversible gate, called the SWAP (S) gate which interchanges the input.

Toffoli's Gate:

In Toffoli Gate (Agarwal, Choudhary, Jangid, & Kasera, 2017), all the inputs that is from1 to (n-1) are mapped to its corresponding outputs. The final output is coordinated by inputs from 1 to (n-1). To upended and pass the nth input make all inputs as 1 else pass original

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output. The first two inputs corresponds to outputs and the third output controlled by first two input and invert it. The truth table has been shown in Table.

MTSG gate:

In MTSG gate (Agarwal *et al.*, 2017) four number of inputs and outputs are used. By this design the one bit full adder is designed.

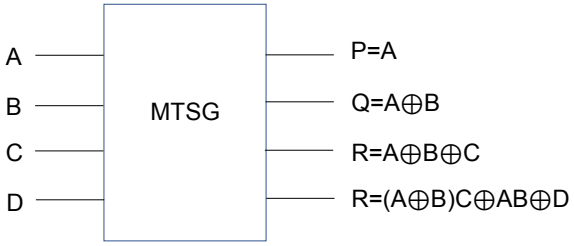

Figure 2. MTSG gate.

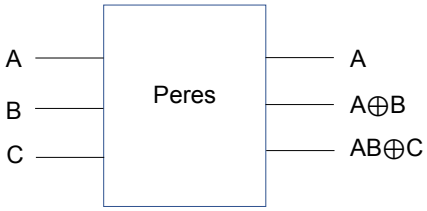

Figure 3. Peres gate.

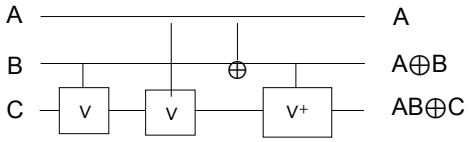

Figure 4. Internal architecture with Peres gate.

Table 2. Peres gate truth table.

A	B	C	P	Q	R
0	0	0	0	0	0
0	0	1	0	0	1
0	1	0	0	1	0
0	1	1	0	1	1
1	0	0	1	1	0
1	0	1	1	1	1
1	1	0	1	0	1
1	1	1	1	0	0

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2. LOOK AHEAD CARRY ADDER

A. CONCEPT OF CARRY GENERATOR

Look ahead carry adder used to *produce* and *circulate* carry. In binary addition when both the inputs are 1, it generates carry and propagate

If either of the input is 1 then A+B propagates in case binary addition. Binary predicate is represented as *P(A,B)*

P (A, B) =A+B

If binary addition, then expression can be represented as:

P'(A, B) =A xor B

Binary operation performs faster than xor. Though we can use P'(A, B) for multiple bit carry look ahead adder.

In Boolean function, P_i represented as propagate, Ci denoted as carry bit and G_i generate binary bit.

Ci+1=Gi+ (Pi.Ci)

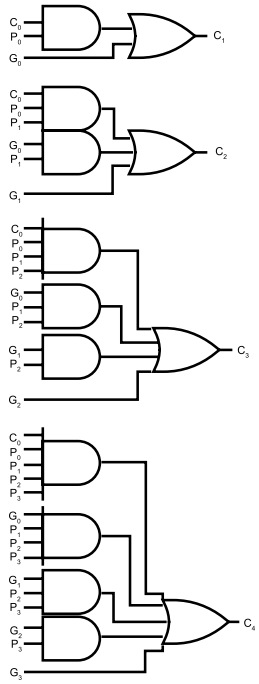

Figure 5. Existing model of carry generator.

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3. PROPOSED ADDER ARCHITECTURES

This deals with the Design and operation of the proposed look ahead carry adder architecture using Peres gate based on the existing adder architecture. The proposed architectures are implemented by replacing the three block's (Peres full adder) Peres gates and peresfull adders with reversible logic gates to obtain the better performance compared to conventional logic.

Design I

In this sector look ahead carry adder using Peres logic is proposed. As we know the Peres logic already, it is pretty much easier to propose this type of adder using the Peres reversible gate. The Peres full adder is already proposed (Somani, Chaudhary, & Yadav, 2016; Lisa, & Babu, 2015).

Whenever the quantum cost of the Peres gate is said to be four and the Peres full adder consist of two Peres gate, which proposes the quantum cost of eight. In addition, the minimal number of reversible logic gates used for proposing a 4 bit look ahead carry adder is 32. This design proposes the 4 bit look ahead carry adder design consist of four sum elements and a carry output.

I. PROPOSED LOOK AHEAD CARRY ADDER

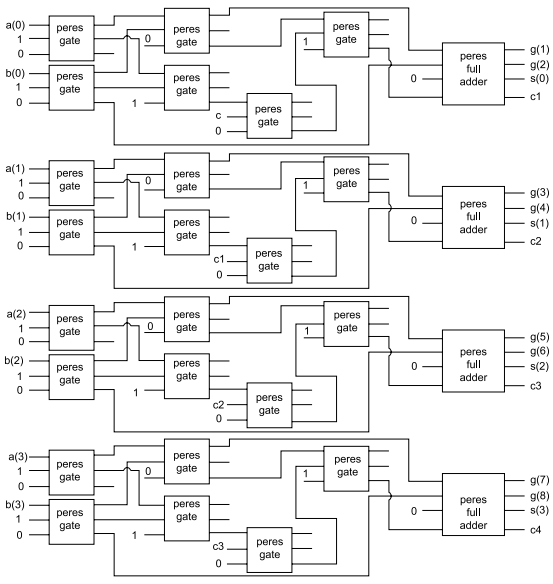

Figure 6. Look ahead carry adder Design 1.

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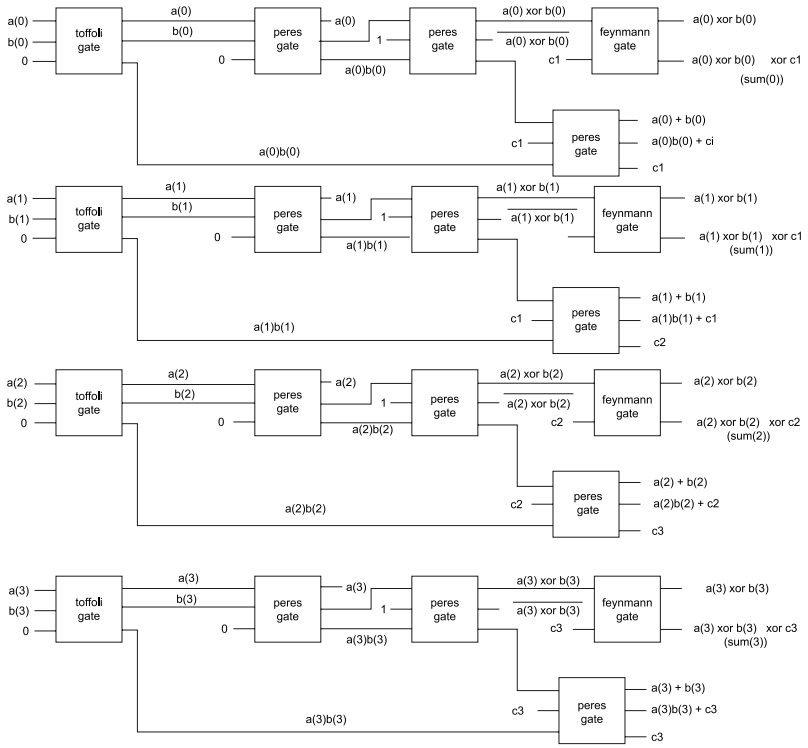

Figure 7. Look ahead carry adder Design 2.

This second design is proposed by using three types of reversible gates (Peres, Toffoli, Feynmann) (Somani *et al.*, 2016) although it is already proposed through the survey that the gates quantum cost (Peres, Toffoli, Feynmann) (Somani *et al.*, 2016) are 4,5 and 1 respectively. By proposing this adder the quantum cost and the count of garbage outputs are also reduced. The above design proposes a design with four sum elements and a single carry output. And this design has a quantum cost of 18 for a single bit adder.

B. PROPOSED CARRY SAVE ADDER

This deals with the designing and optimization of the carry save adder by replacing the conventional logic gates by the reversible gates. By considering the minimal quantum cost containing design as the best design.

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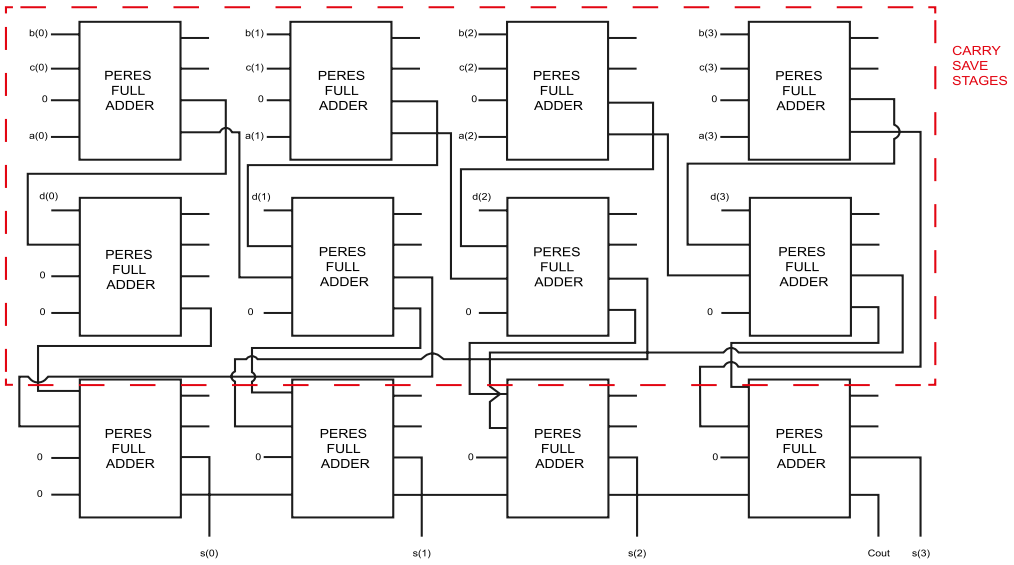

Figure 8. Design 1.

Proposed 4 bit carry save adder is designed Peres full adder. Source: (Somani *et al.*, 2016).

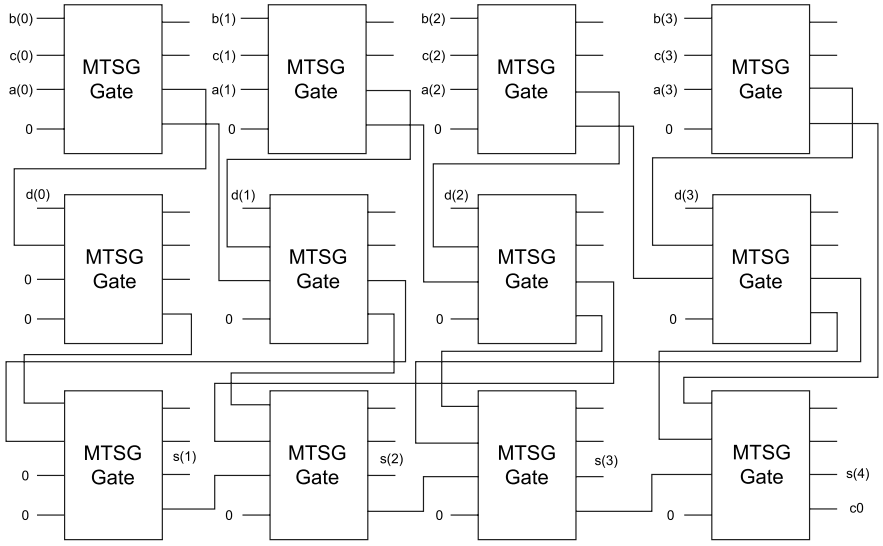

Figure 9. Design 2.

This design proposed by using the MTSG gates.

4. SIMULATION RESULTS

Proposed reversible adder circuit is more proficient than existing method. Based on the comparative analysis, proposed design can be easily realized. In existing design, logic gate

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used instead of that in proposed work reversible gate such as Peres used to understand the circuit. The circuit realized using reversible Peres gate to reduce the logical calculation. Also in terms of hardware complexity proposed work is efficient than exiting circuit.

All the simulations have been done using XILINX 9.2i and Model sim Altera 6.3g_p1.

SIMULATION RESULTS OF PROPOSED ARCHITECTURE

Design I

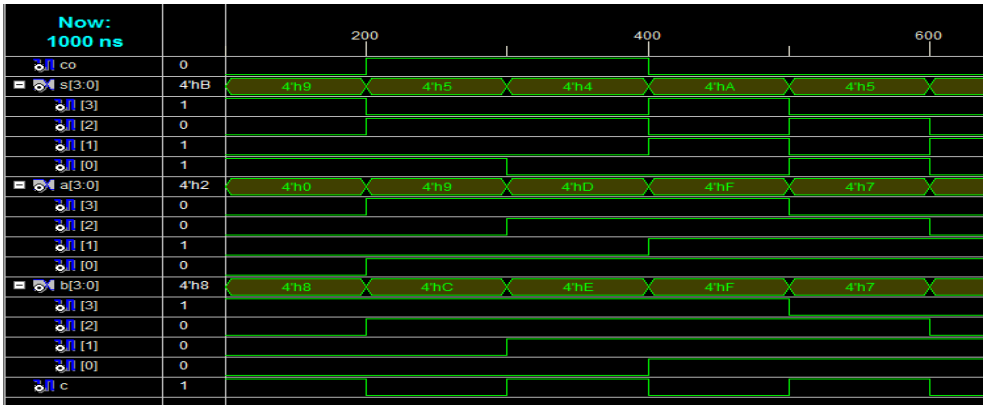

Figure 10. Proposed Design 1 Look ahead carry adder simulation results.

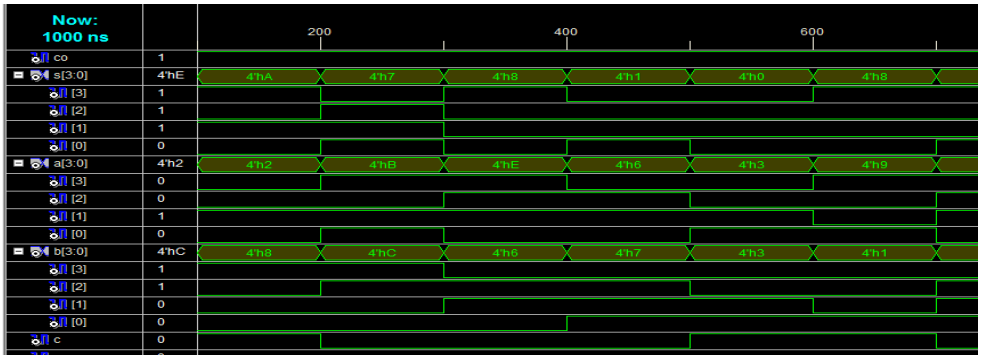

Figure 11. Proposed Design 2 Look ahead carry adder simulation results.

The above Figure shows the results of the proposed reversible look ahead carry adder for three different inputs. the inputs to the adder is two 4-bit binary coded decimal numbers named a and b and carry Cin.

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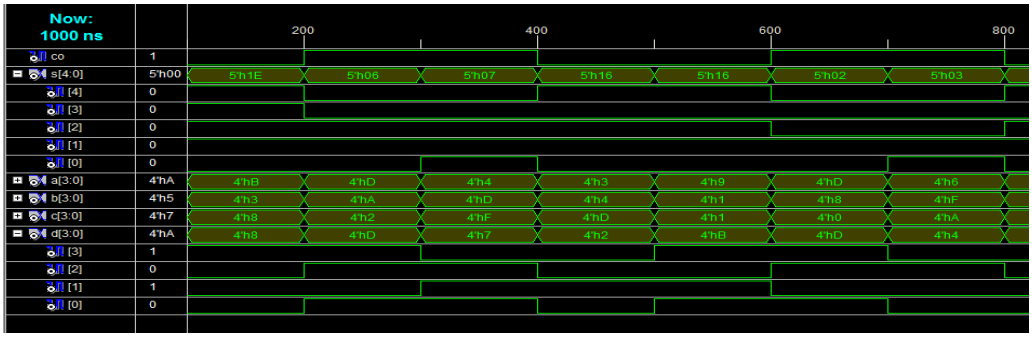

Figure 12. Proposed design 1 carry save adder simulation results.

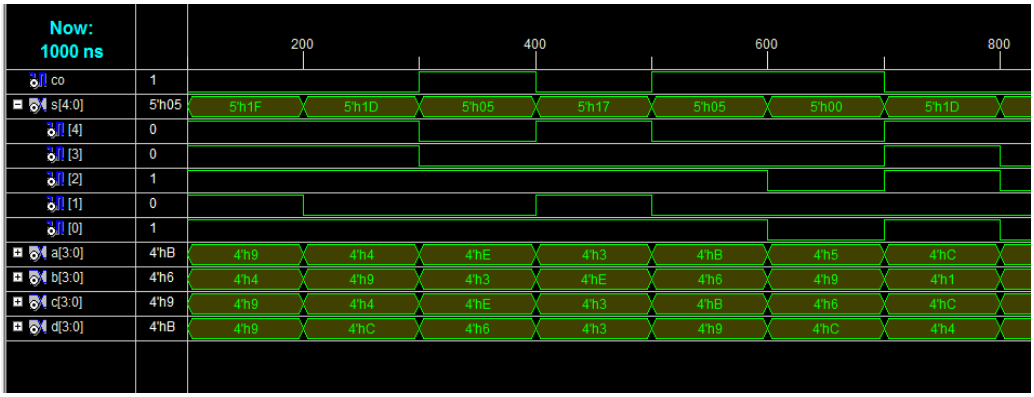

Figure 13. Proposed design 2 carry save adder simulation results.

HARDWARE AND SOFTWARE USED

All simulations have been done using Xilinx ISE 9.2i.

5. APPLICATIONS

Applications based on reversible logic concept are listed. (1) Nano Computing (2) Spacecraft (3) Bio Molecular Computations (4) Quantum Computing (5) Low power CMOS.

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6. CONCLUSION

Look ahead carry adder is designed with reversible logic gates. Proposed design optimized with existing design in terms of reversible gate operations.

Table 3. Carry look ahead adder optimization results.

Design	No. of reversible gates used	No. of garbage outputs	Quantum cost	Time delay
Design 1	32	40	128	14.33ns
Design 2	20	20	72	12.275 ns

Table 4. Optimization table of carry save adder.

Design	Nº.of reversible gates used	Nº.of garbage outputs	Quantum cost	Time delay
Design 1	24	24	96	19.219 ns
Design 2	12	24	72	15.873 ns

Reversible circuit design strategy is used to reduce the complexity and circuit cost. Distinguish the circuit with reversible systems, which performs more number of complex operations. Based on the reversible circuit design main factors like garbage outputs, quantum cost and delay of the circuit reduced. In addition, circuit complexity reduced by reducing the reversible gates. This work customs basic step in constructing complicated reversible systems,which can perform more comple x operations. Based on logical synthesis alternative design can be implemented. To decrease system design and manufacturing cost VLSI system implemented with one type of modular building. To reduce quantum cost and gates count, further design can be implemented using other reversible logic gates.

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